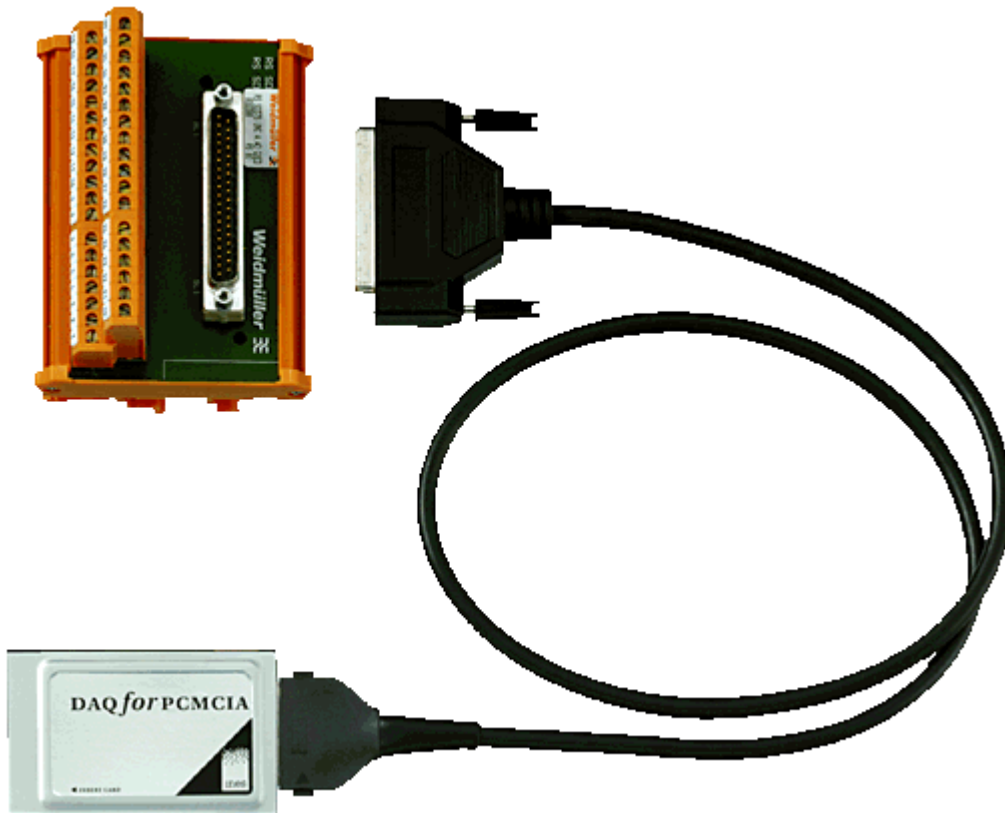


Data Acquisition Card Hardware manual



12 bit data acquisition PC-Cards

DAQ i108, DAQ i116, DAQ i250, DAQ i508, DAQ i516, DAQ i608 and DAQ i616

with 8 or 16 input channels and 100kHz..625kHz sample rate

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Card's function

To say very simple, the cards provide a means to convert analog input voltages into digital data. Second, a facility for transferring digital data is built-in.

The conversion from analog input voltages to digital data is performed by a successive approximation converter. This type of converter approximates the analog input voltage level by using a D/A converter and a comparator.

The converter uses 12 steps (1 step for 1 bit of resolution) to track the input signal. First the D/A converter creates an output voltage that's 50% of the input voltage range. The comparator tells if the input signal is higher or lower than the D/A output voltage. Then the D/A output is adjusted to the input voltage in finer and finer steps. Each step results in a higher/lower decision and in one bit of resolution. After 12 steps, the process is finished and the 12 bit data word is ready.

Digital data can be transferred with 8 signals, that means 8 bits. The direction can be switched by software for each signal.

Acquisition modes

The cards can acquire data in a variety of modes:

Single conversion mode

The card takes a single reading without trigger. This is the mode intended for streaming data into the PC at very low rates.

As soon as software activates the RUN bit in SUR1 register, a single conversion occurs. The PC reads the sample out. The card automatically clears the RUN state, so it is ready for the PC to set the next conversion. The time between conversions is totally software-controlled. Remember to pre-clear the READ & WRITE POINTERS (and do not try to set any pre-trigger) prior to commanding a single conversion (this ensures that the process stops immediately after one conversion rather than filling the whole SRAM buffer).

This mode works for one channel only! It is used in cases where only a single measurement on a single channel is sufficient and the result is needed immediately.

Trigger mode

In this mode the card waits for a predefined event and then stores data up to the FIFOs size.

A pretrigger count can be set, for samples before the occurrence of the trigger event are recorded.

The card is set up with trigger threshold and edge. The READ and WRITE POINTERS are put into a known starting state. The pre-trigger depth is configured. The system is

set into RUN mode but with trigger disabled. It starts taking samples into the internal FIFO buffer. After some elapsed time, software sets ENTRIG active to "arm" the system. Now the card waits until the incoming sample data meets the trigger requirements. The FIFO buffer is circular so all the time that the card is waiting for trigger samples are being stored away. When triggered, the READ POINTER freezes. Conversions continue until the WRITE POINTER equals the READ POINTER. Then the system halts and generates an interrupt, depending on the setting of the SELCTRD bit in SUR2. The PC reads out the sample data from the SRAM for display / processing.

The trigger conditions are set by

- trigger mode: Bits TREDGE and LVL in SUR2 register
- trigger level: Byte in TRIDTHRESH

The number of possible conditions is a combination of the 3 parameters:

Trigger Mode	Input signal
greater than trigger level	$U_i(t) > U_t$
less than trigger level	$U_i(t) < U_t$
negative (falling) edge at trigger level	$U_i(t-1) > U_t$ and $U_i(t) < U_t$
positive (rising) edge at trigger level	$U_i(t-1) < U_t$ and $U_i(t) > U_t$

$U_i(t)$: Input voltage at sample time at converter

U_t : Trigger level

$U_i(t-1)$: Input voltage at previous sample time at converter

The resolution of the trigger circuit is 8 bit (instead of cards 12 bit). For the maximum input voltage range of +/- 10V the trigger resolution is around 80mV. Do not be alarmed if the card triggers not exactly at the set trigger level.

Using external trigger input

The acquisition is started by a pulse at external trigger input line (TRIGGER). Pulse the line low for a time of at least one sample period. The line is pulled to +5V level by an internal 10k resistor.

Make sure that the trigger condition that must be set will never trigger:

The card triggers never if trigger mode is set to greater than level and the level is maximum input level.

See the section Selecting trigger conditions for reference.

Continuous acquisition (data stream) mode

The card starts taking samples until it is stopped. There is no triggering. The card can be stopped manually, but it also stops itself if the FIFO buffer overflows. This mode results in a continuous data stream. So fast reading of the data is essential!

Only very fast computers can handle the maximum sample rate of 650kHz (DAQ i608/i616) because a constant throughput of 1.3MByte per second is needed.

As soon as software activates the RUN bit in SUR1 register, the FIFO buffer starts to fill. The user program must empty the SRAM at a rate at least equal to the rate at which it is

being filled. An interrupt can be generated at 1/4 or 1/2 full. If an overrun occurs, i.e. the WRITE POINTER catches the READ POINTER up, the card will stop automatically.

If an Intel 80x86 processor is used, use the "REP INSW" instruction to get high speed.

A/D converter binary data format

The A/D converter produces 2's complement 12 bit output codes when in Bipolar mode and "true binary" 12 bit codes when in Unipolar mode. Table 3.2-1 summarises the codes.

Analog input voltage	A/D converter binary output			
	Bipolar, from -full scale to +full scale		Unipolar, from 0 to +full scale	
	Binary	Hex	Binary	Hex
Full scale	011111111111	7FF	111111111111	FFF
Full scale -1 LSB	011111111110	7FE	111111111110	FFE
...
0 +1LSB	000000000001	001	000000000001	001
0	000000000000	000	000000000000	000
0 - 1LSB	111111111111	FFF	Out of A/D range	
- Full scale + 1LSB	100000000001	801	Out of A/D range	
- Full scale	100000000000	800	Out of A/D range	

- The size of the LSB step depends on the input range selected and whether you are operating in Unipolar or Bipolar mode.
- Do not mix up the terms 'Bipolar / Unipolar' and 'Single ended / Differential'!

20 different input ranges can be set. The gain is programmed using the top four bits of SETUP REG 1 (GS0..3). The following table summarises the gains and input ranges available:

GS0..3 bits in SUR1 register	Bipolar input range	Unipolar input range
0x0	± 0.625	0V...1.25V
0x1	± 1.25	0...2.5V
0x2	± 1.875	0...3.75V
0x3	± 2.5	0...5.0V
0x4	± 3.125	0...6.25V
0x5	± 3.75	0...7.5V
0x6	± 4.375	0...8.75V
0x7	± 5.0	0...10.0V
0x8	± 5.625	Not available
0x9	± 6.25	Not available
0xA	± 6.875	Not available

0xB	± 7.5	Not available
0xC	± 8.125	Not available
0xD	± 8.75	Not available
0xE	± 9.375	Not available
0xF	± 10.0	Not available

Trigger

The DAQ I508 will not trigger unless Bit 1 of SETUP REG 1 is low. This allows software to "arm" the DAQ I508 only when it is appropriate to do so i.e. after some start up condition or when the user has signalled that the system should arm ready to capture an event.

Trigger threshold

An 8-bit 2's complement OR "true binary" trigger threshold value. This is compared against the top 8-bits of the 12-bits of A to D data to decide when to trigger the card. The value loaded into the threshold register MUST be appropriate to the conversion mode selected: 2's complement for Bipolar, "true binary" for Unipolar.

In C/C++ the threshold is calculated as a SHORT INT in the following way:

Bipolar mode:

$\text{TRIGBYTE} = \text{ROUND}(128 * (\text{Vtrig}/\text{Vfs}));$ /*Vfs = full scale input voltage */

Unipolar mode:

$\text{TRIGBYTE} = \text{ROUND}(256 * (\text{Vtrig}/\text{Vfs}));$ /*Vfs = full scale input voltage */

Remember that the value loaded into the trigger threshold register varies depending on the full scale input range selected via GS0..3.

When a trigger event occurs while the ENTRIG is low in SUR1 register, the READ POINTER is frozen but the WRITE POINTER continues to run. Once the READ and WRITE POINTER are equal (i.e. the buffer is full) the DAQ I508 halts and sets the RUN bit in SETUP REG 1. This can be polled in software to see when the card has halted. If enabled via the HOST, this will also cause an interrupt. Software can also check the TRIGGER STATUS via Bit 5 of SETUP REG 1: a 1 indicates TRIGGERED.

Triggering is only used in BURST mode.

Pretrigger

Before performing an acquisition in trigger mode, the WRITE POINTER must be pre-decremented at least once by software (i.e. 2 bytes). This will give a pre-trigger depth of 1 conversion. To make the pre-trigger depth greater simply pre-decrement the WRITE POINTER extra times, each write to the DECW register will give one conversion more pre-trigger. So to set 200 conversions for the pre-trigger depth, pre-clear the pointers (3.3.2) and then write 200 times to the DECW port (don't care data).

Remember that you must control the RUN and ENTRIG bits correctly to ensure that the pre-trigger buffer actually holds valid conversion data: the DAQ I508 could trigger before

conversion results have been written into the whole pre-trigger area of SRAM. The rule is to set the DAQ I508 into RUN mode but with ENTRIG off, in software wait a minimum of $(t \times n)$ seconds before enabling trigger (t is the sample period, n is the pre-trigger depth in conversions).

Reading FIFO data

FIFO data is accessed at I/O address $\langle \text{base}+2 \rangle$. Each read by the PC will fetch data and decrement the READ POINTER. If the card has halted after an acquisition in trigger mode, then the READ pointer must be released to read out the A to D data. This is achieved by setting SINGLE bit in SUR2 register. Be sure to return this bit to zero before attempting to do further acquisitions.

FIFO data can be read as bytes or words. If reading bytes, read two bytes to make a 16-bit value; the data is stored in the bottom 12 bits. If reading words, read 1 word to get a 16-bit value. The word wide transfer will be broken into 2 byte wide transfers automatically by the PCMCIA controller. Word access throughput is faster than byte access throughput. The PCMCIA controller should be configured with an 8-bit wide IO window running from $\langle \text{base} \rangle$ to including $\langle \text{base}+3 \rangle$

Note that the top 4 bits of the FIFO data hold the MUXSEQ count of the conversion.

Sample rate

The sample rate is programmed via a 14-bit divider, accessed as an 8-bit register (DIVLO) and a 6-bit register (DIVHI). The clock divider runs at 5MHz. Additionally, there is an extra control bit that allows subtraction of a $\frac{1}{4}$ clock period from the divider. This is located in SUR1 register and called "!TIMING". The purpose of this bit is to allow a finer frequency resolution and additional frequencies to be obtained.

The formula for the calculation of available sample rate is:

- At sample rates less than 50kHz steps are finer than 1 per cent of the sample rate.
- At higher rates the 'even' frequencies 500kHz, 250kHz, 200kHz, 125kHz, 100kHz, 62.5kHz and 50kHz are available (also repeating each decade).
- Note that the built-in one-pole lowpass filter limits the bandwidth. You can simply change the cutoff frequency by adding a series resistor. The 3db cutoff frequency with an additional resistor R is given (approximately) by: $f = 1 / (2.011 \times 10^{-9} \times (2000+R))$

The calculation for the two data bytes is given by:

!TIMING=1: $\text{DIVHI} = (\text{round}(1/(\text{FSample} \times 200\text{E-}9)) - 2) \gg 8$, $\text{DIVLO} = (\text{round}(1/(\text{FSample} \times 200\text{E-}9)) - 2) \& 255$;

!TIMING=0: $\text{DIVHI} = (\text{round}(1/(\text{FSample} \times 200\text{E-}9)) - 1.75) \gg 8$, $\text{DIVLO} = (\text{round}(1/(\text{FSample} \times 200\text{E-}9)) - 1.75) \& 255$;

[FSample]=Hz

For the DAQ i508/i516 and DAQ i608/i616 the input bandwidth of the card is restricted to around 250KHz to aid with anti-aliasing requirements. For the DAQ i250 it is limited to around 120KHz. If slower sample rates are used and signals greater than the Nyquist rate are present in the input signal, some form of off card low-pass filtering may be required. This filtering can be as simple as placing resistance in line with the input signal. When adding series resistance, don't forget that you will also tend to degrade the card's accuracy and induce offset errors due to bias currents etc

Control of input channel multiplexer

There are 8 input channels to the DAQ ix08 and 16 to the DAQ ix16. The channels can be used either in single ended mode i.e. number of input channels equals 8 or 16 OR they can be set to work in true differential mode giving 4 channels (DAQ ix08) or 8 channels (DAQ ix16). Refer to the pinout table for details of which channels are "differential pairs".

The multiplexers are controlled by a 4-bit address generated by an up counter. The register MUXSEQ controls the start and end channel of the counter. The register is organised as 2 values at 4-bit each. The counter is preloaded with bits0..3 of the register (that the starting channel) and counts up to bits4..7 (last channel of the sequence). It then resets to the starting channel again.

Before starting conversions the counter MUST be initialised with the start address from the MUXSEQ register by writing setting the SELCTRD bit in SUR2 and then writing don't care data to the CLRCT register.

Remember that

- this will undo any setup for pre-trigger! that you may have made so the order of events is important ii)
- to set SELCTRD low again
- that setting SELCTRD to a 1 will clear any pending interrupt

After each conversion, the counter is incremented by one. The MUXSEQ register does not change during conversions; it provides permanent storage of the start and end addresses.

The bit significance of the 4 bit counter changes depending whether the card is in single ended or differential mode. In single ended mode all four bits are used to cycle through the input channels in the order in which they are numbered i.e. A1, A2, A3 etc. In differential mode, the MSB of the counter is not used. When loading the MUXSEQ register and operating in differential mode be sure to set both bit3 and bit7 to zero (i.e. the MSBs of the start and end addresses). In differential mode the 3 bit count value is used to cycle channels in pairs i.e. A1&A5, A2&A6, A3&A7 etc.

When the card stores the sample data into FIFO it also saves the mux counter value for the conversion in the top four bits of the 16-bit data word.

The MUX address changes approximately 100ns after the track and hold enters hold mode for the current conversion.

Examples of most used settings:

- MUXSEQ=0x00: One channel. Input channel A1 is scanned. If differential mode is turned on, the channel pair A1 (+ input) and A5 (- input) is scanned. Again, it results in one channel.
- MUXSEQ=0xF0: Start channel is 0, that means A1, end channel is 15, that means A16. Channel scan sequence is A1, A2, A3, A4, A4, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16 and from the beginning. Note that this setting is invalid if differential mode is turned on! Also it works only for cards with 16 input channels
- MUXSEQ=0x70: Start channel is 0, that means A1, end channel is 7, that means A8. Channel scan sequence is A1, A2, A3, A4, A4, A6, A7, A8 and from the beginning. If differential mode is turned on (cards with 16 input channels only!) the sequence (A1+ A5-), (A2+ A6-), (A3+ A7-), (A4+ A8-), (A9+ A13-), (A10+ A14-), (A11+ A15-), (A12+ A16-) is scanned.
- MUXSEQ=0x10: Two channel scanning: A0 A1 A0 A1...

Differential input vs. single ended input

As default, all voltages applied to the input channel are measured relative to card's ground (more precisely: to the AGND pin). Sometimes voltages that shall be measured do not share a common ground. In this case, the card can be switched to differential inputs. In this mode, two input channels become 1 differential input channel, one channel, i.e. A1 becomes '+' input, and A5 becomes '-' input. See the Connector pinout for further reference on pin assignments.

Using differential inputs, the signals may differ in ground potential relative to each other and to the card, however, the difference *must not* be greater than the maximum input voltage range $\pm 10V$, relative to card's ground at AGND. If this restriction is not observed, the input signal may be clipped during A/D conversion, so that wrong readings occur. In the worst case, the built-in protection circuit becomes active if the voltage difference is greater than 35V. Finally, the card can be damaged! So, always check the relative voltage to card's ground at pin AGND!

Sleep mode

The cards can be put into a power-down mode. The internal DC-DC converters, oscillator and A/D converter are shut down. The analogue part of the card will not function in this mode. When enabling the card so that it is coming out of sleep mode, allow at least 2 seconds for the power to stabilise before taking any measurements.

The card powers up in sleep mode and enters sleep mode after a hard or soft reset. The !SLEEP bit in SUR1 controls the sleep state.

- Note that after powering up the card and bringing the card out of sleep, the RUN state should be set to active then back to inactive. This allows internal clock generation to stabilise prior to taking any ADC readings. Failure to do this can show as a "bad" first sample from the ADC directly after power-up.

INTERRUPTS

The DAQ I508 can generate interrupts if the HOST enables the PC-Card IREQ signal to a PC interrupt channel. Using interrupts is a convenient and efficient means of keeping

track of what the card is doing. Interrupts work differently depending on which mode the card is in:

- In Trigger mode, an interrupt can be generated after the FIFO buffer has filled.
- In Continous mode, an interrupt can be created, if
 - the buffer is full - that's not useful
 - if the buffer is half full - most useful
 - if the buffer is quarter full - also useful
 - one conversion took place - that's useful if low samples are used, since one does not have to wait until the buffer is filled, it may take up to 8 seconds.
- In Single Conversion mode, ignore any interrupts.

Alternatively, the interrupt state can be polled for in software, you do not have to use interrupts. This is because the state of the internal Flip-Flop that latches the interrupt state can be read via the IREQ bit in IODIR register.

The interrupt is latched. It must be cleared before another interrupt can be generated. To clear it read from the FIFO buffer. It can also be cleared by a soft or hard reset or by pulsing the SELCTRD bit in SUR2 register low-high-low.

Note that

- leaving the SELCTRD bit high will block all interrupt events and will stop the multiplexer counter (MUXSEQ register) from counting.
- using the CLRCT port to reset the internal counters may cause an artificial IREQ event when in FIFO mode. Use the SELCTRD bit to clear this.

Digital I/O lines

There are 8 digital IO lines which can be used for general control / monitoring.

The bottom 4 bits of the IODIR register are used to configure the IOPINs as inputs or outputs. Bit 0 controls the direction of IOPIN0, bit 1 controls IOPIN1, bit 2 controls both IOPIN2&3, and bit 3 controls IOPINs 4,5,6 and IOPIN7.

Setting a bit high enables the pin/group of pins as outputs. The data to / from the pins is read via the IODATA register as byte and logically the bit position in the byte corresponds to the particular IOPIN that is addressed i.e. Bit 4 IOPIN4.

The standard card has a built-in bidirectional 8 bit I/O port that is TTL-level compliant.

The design does not offer all 256 possible combinations for input and output:
IOPIN 0 and IOPIN 1 can be set freely.
IOPIN 2&3 can only be set as input or output together; this is for IOPIN 4..7 too.

These patterns are valid:

Valid Patterns															
in Hex:	0	1	2	3	C	D	E	F	F0	F1	F2	F3	FC	FD	FE

in decimal:	0	1	2	3	12	13	14	15	240	241	242	243	252	253	254
Port															
IOPIN 0	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I
IOPIN 1	I	I	O	O	I	I	O	O	I	I	O	O	I	I	O
IOPIN 2	I	I	I	I	O	O	O	O	I	I	I	I	O	O	O
IOPIN 3	I	I	I	I	O	O	O	O	I	I	I	I	O	O	O
IOPIN 4	I	I	I	I	I	I	I	I	O	O	O	O	O	O	O
IOPIN 5	I	I	I	I	I	I	I	I	O	O	O	O	O	O	O
IOPIN 6	I	I	I	I	I	I	I	I	O	O	O	O	O	O	O
IOPIN 7	I	I	I	I	I	I	I	I	O	O	O	O	O	O	O

I : Input

O : Output

That means: from zero to all 8 pins for input or output can be defined, but the set of pins is fixed.

Possible sources of measurement error

Distorted signal using differential inputs

When using Differential input mode, it may happen that the input signal looks like distorted.

This effect is caused by a signal that is out of the card's input voltage range, relative to card's ground.

The card provides differential input, but the differential input signal must be within the input voltage range of +/-10V, relative to card's ground.

Hint: Try connecting a 1MOhm resistor from one input pin to AGND, i.e. 1+ to AGND.

The signal shall return to its expected waveform, because it does not 'float' any longer.

Ground loops

Can be caused when the source's ground is connected via the cable and to the shield on the PC-Cards connector. Most often, the shield is connected to the PC's housing. For safety reasons, the housing is connected to earth via the power lines. If the source's ground is connected to earth too, and if these two potentials of earth are not equal, current will flow in the analogue ground wire. This will cause voltage offsets due to cable losses. Avoid such loops. Do not connect the shield to any other terminal. In the DAQ card the shield is already connected to the PC's housing.

Noise

Avoid long connections to the analogue inputs. If you can't avoid them, try differential mode measurement. If the same noise is introduced on both input lines, it may become non-existent.

Some extra noise is introduced by the card itself with the voltage references, the analogue input amplifier and the power supply. The power rails inside the card are designed for maximum suppression of noise and spikes, but the PC environment with lots of digital switching circuits is not ideal analogue circuits. A battery powered Notebook provides 'cleaner' power than a desktop PC with switching power supply.

Temperature drift

At the time the computer is turned on, the card starts heating itself up until a thermal balance is reached. In addition, heat from devices nearby affect card's temperature. During that time of approximately 15 minutes, readings are unstable. The total card's temperature drift is the sum of the drift of the card's internal amplifier and the drift of the voltage reference.

Register interface

The cards decodes addresses in the PCMCIA attribute memory space like this:

0x0-0x3FF	CIS (Card information structure)
0x400-0x7FF	PCMCIA Configuration option register, repeats every byte
0x800-0xBFF	CIS, mirror from 0x0-0x3FF

The Configuration option register is used as a master enable, as defined by PC-Card standard V2.01. That is, when a valid config is written in bits0..5 the card's I/O interface may function. Until this has happened, the card's I/O interface is disabled. A value of 0 for the Configuration option register will disable the card (this is the state after a reset). Valid values are 0x01 0x05. See the section on the Configuration option register for details of the various modes.

Bit7 of the COR acts as a soft reset when set (the reset does not clear bit7 but a subsequent write to the config register to return bit 7 to zero should not attempt to load data into bits 6..0 of the register as they will still clear. This should be done as a separate write operation.)

Configuration option register

The cards uses the Config Option Register or COR that is defined by the PC-Card standard to enable a particular mode. The COR is at offset 0x400 in attribute space (defined in CIS) and is 8-bits wide read/write. It is organised as follows:

Config option register value	Function
0x0	Card is disabled
0x1	Trigger mode
0x5	Continuous acquisition mode
0x80 0x81 0x85	Card software reset

Card registers

All cards functions are accessed via three I/O ports (starting at <base> address as mapped by the host controller). Address A0 and A1 are decoded, giving an Index Register (IR) at <base>+0, a Data Register (DR) at <base>+1 and the FIFO port at <base>+2&3. The IR is 8-bits wide and is write only (you can't read back what you have written). The IR selects which internal register is to be read/written via the DR (cf 82365

PCIC). The DR is also 8-bits wide. It is the job of the host socket controller to map the IR, DR and SRAM data registers into the system's IO space starting at IOBASE and ending at IOBASE+3.

Address offset in byte from <base>	Function
+0	IR - Index register
+1	DR - Data register
+2	FIFO (byte access)
+3	FIFO (word access)

For accessing an on-card register, one must perform these steps (exemplary read access to SUR2):

- Write byte 0x1 (offset of SUR2 register) to <base> (IR register)
- Read byte from <base>+1 (DR register). This is the contents of the SUR2 register

The following table shows the **indexes** of the various registers in the card:

Index register (IR) value	Data register (DR) write	Data register (DR) read
0x0	SUR1 - Setup register 1	
0x1	SUR2 - Setup register 2	
0x2	IODATA - Digital I/O port data register	
0x3	IODIR - Digital I/O port direction register	
0x4	DIVLO - Lower byte of clock divider	ADDRCTLO - Lower byte of Read or Write pointer (selected by SELCTRD bit in SUR1)
0x5	DIVHI - Higher byte of clock divider	ADDRCTHI - Higher byte of Read or Write pointer (selected by SELCTRD bit in SUR1)
0x6	MUXSEQ - Input channel multiplexer control	- No read back -
0x7	TRIGTHRESH - Trigger level	- No read back -
0x8	- Not used -	
0x9	CTLEN - Control length of FIFO	- No read back -
0xA	- Not used -	
0xB	- Not used -	
0xC	- Not used -	
0xD	DECR - Decrement Read pointer (any access decrements)	
0xE	DECW - Decrement Write pointer (any access decrements)	
0xF	CLRCT - Clear multiplexer counter and read and write pointer (any access clears/resets)	

Register bit assignment

- All BINARY values are shown with MSB leftmost
- All bits with a leading '!' are active '0'.
- '0' means TTL low level, '1' means TTL high level.

SUR1 (IR = 0x0) - Setup register 1

Bit	Write	Read	Reset state
0	!RUN =0: Start taking conversions or start a single conversion	!RUN	1
1	!ENTRIG =0: Enable triggering and arm the card in trigger mode	!ENTRIG	1
2	!TIMING =0: Enable a ¼ clock period subtraction in the clock divider	!TIMING	1
3	!SLEEP =0: Put the card into power-down mode.	!SLEEP	0
4	GS0 (LSB) - GS0...GS3 affect the input voltage range setting	GS0	0
5	GS1	GS1	0
6	GS2	GS2	0
7	GS3 (MSB)	GS3	0

SUR2 (IR = 0x1) - Setup register 2

Bit	Write	Read	Reset state
0	IBITSEL0 (LSB)	IBITSEL0	0
1	IBITSEL1 (MSB) - Interrupt generation selector (only applies in FIFO mode): =00: Interrupt when buffer full =01: Interrupt every ½ buffer full =10: Interrupt every ¼ buffer full =11: Interrupt every conversion	IBITSEL1	0
2	BIPOLAR: =1: Use bipolar input voltage range. =0: Use unipolar input voltage range	BIPOLAR	0
3	SINGLEEND: =1: Single ended (grund referenced) input, =0: Differential input	BIPOLAR	0
4	TREDGE 1: >level or positive edge, =0: <level or negative edge	TREDGE	0
5	LVL: =1: Trigger level mode, =0: Trigger edge mode	LVL	0
6	SELCTRD: =0: ADDRCTL0/HI registers read READ pointer, =1: ADDRCTL0/HI registers read WRITE pointer, interrupts are blocked Pulse 0-1-0 to clear interrupt, then set to 1 to block interrupts	SELCTRD	0

7	SINGLE: =0: FIFO mode: Continuous mode =1: FIFO mode: Single conversion mode, perform single conversion if !RUN=0 Trigger mode: Release READ/WRITE pointers to read FIFO data	SINGLE	0
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IODATA (IR = 0x2) - Digital I/O port data register

Bit	Write	Read	Reset state
0	IOPIN0 (LSB) - Set level at port pin	IOPIN0 - Read level at port pin	0
1	IOPIN1	IOPIN1	0
2	IOPIN2	IOPIN2	0
3	IOPIN3	IOPIN3	0
4	IOPIN4	IOPIN4	0
5	IOPIN	IOPIN5	0
6	IOPIN	IOPIN6	0
7	IOPIN7 (MSB)	IOPIN7	0

IODIR (IR = 0x3) - Digital I/O port direction

Bit	Write	Read	Reset state
0	IODIR0 =0: IOPIN0 is input =1: IOPIN0 is output	IODIR0	0
1	IODIR1 =0: IOPIN1 is input =1: IOPIN1 is output	IODIR1	0
2	IODIR2 =0: IOPIN2,3 are inputs =1: IOPIN2,3 are outputs	IODIR2	0
3	IODIR3 =0: IOPIN4...7 are inputs =1: IOPIN4...7 are outputs	IODIR3	0
4	-	!IREQ =0: Interrupt is pending, =1: Interrupt inactive	1
5	-	TRIGGERED =0: Not triggered, =1: Trigger event occurred while card is running (!RUN=0) and armed (!ENTRIG=0)	0
6	-	-	0
7	-	-	0

DIVLO / ADDRCTL0 (IR = 0x4) - Lower byte of clock divider / Lower byte of READ/WRITE pointer into FIFO buffer

This register is 8 bits wide. If it is written to, the clock divider value is returned. If it is read, the READ or WRITE pointer is read, depending on the SELCTRD bit in SUR1

register.

DIVHI / ADDRCTHI (IR = 0x5) - Higher byte of clock divider / Higher byte of READ/WRITE pointer into FIFO buffer

This register is 8 bits wide. If it is written to, the clock divider value is returned. If it is read, the READ or WRITE pointer is read, depending on the SELCTRD bit in SUR1 register.

MUXSEQ (IR = 0x6) - Input channel multiplexer sequencer control

Bit	Write	Read	Reset state
0	MUXSEQ0 - MUXSEQ0...3 set the start channel of the acquisition	- Write only -	0
1	MUXSEQ1	- Write only -	0
2	MUXSEQ2	- Write only -	0
3	MUXSEQ3	- Write only -	0
4	MUXSEQ4 - MUXSEQ4...7 set the end channel of the acquisition	- Write only -	0
5	MUXSEQ5	- Write only -	0
6	MUXSEQ6	- Write only -	0
7	MUXSEQ7	- Write only -	0

TRIGTHRESH (IR = 0x7) - Trigger level

Contains 8 bit trigger value. This register is write-only. Values can't be read back!
Default setting after reset: 0x00

CTLEN (IR = 0x9) - Control length of FIFO buffer

7 bit value that controls the active length of the FIFO buffer. It is used in trigger mode to set the number of captured samples. This register is write-only. Values can't be read back! Only the following settings are valid:

Value	Function / Number of samples
0x00	128 samples, 256 byte length (default setting after reset)
0x01	256 samples, 512 byte length
0x03	512 samples, 1024 byte length
0x07	1024 samples, 2048 byte length
0x0F	2048 samples, 4096 byte length
0x1F	4096 samples, 8192 byte length
0x3F	8192 samples, 16384 byte length
0x7F	16384 samples, 32768 byte length. Required setting for FIFO mode (continuous acquisition)!

DECR (IR = 0xD) - Decrement READ pointer

Any access to this register will decrement the READ pointer by one. Read or write access doesn't care.

DECW (IR = 0xE) - Decrement WRITE pointer

Any access to this register will decrement the WRITE pointer by one. Read or write access doesn't care.

CLRCT (IR = 0xF) - Clear multiplexer counter and READ/WRITE pointers

Any access to this register resets the multiplexer counter to the value set in MUXSEQ register and clears the READ and WRITE pointer to a value of 0x7FFF.

- Clearing the counters in continuous acquisition (FIFO) mode may result in an interrupt. In advance set the SELCTRD bit in SUR2 register to block the interrupt and pulse it to reset the interrupt.

Connector pinout

directly at the PC-Card. The table shows the pinout of the 32 way shielded connector directly at the PC-Card.

The connector type is: HIROSE NX30TA-32PAA+NX-32TA-CV1+NX-32T-BS

There are also cables available, see below.

Pin	Function	Input channel number in mode	
		single ended / ground referenced	differential
1	Analog input channel A1	1	1+
2	Analog input channel A5	5	1-
3	Analog input channel A2	2	2+
4	Analog input channel A6	6	2-

5	Analog input channel A3	3	3+
6	Analog input channel A7	7	3-
7	Analog input channel A4	4	4+
8	Analog input channel A8	8	4-
9	Analog input channel A9 ⁽¹⁾	9	5+
10	Analog input channel A13 ⁽¹⁾	13	5-
11	Analog input channel A10 ⁽¹⁾	10	6+
12	Analog input channel A14 ⁽¹⁾	14	6-
13	Analog input channel A11 ⁽¹⁾	11	7+
14	Analog input channel A15 ⁽¹⁾	15	7-
15	Analog input channel A12 ⁽¹⁾	12	8+
16	Analog input channel A16 ⁽¹⁾	16	8-
17	AGND - Analogue ground	-	-
18	DGND - Digital ground only	-	-
19	IOPIN0 (I/O bit 0)	-	-
20	IOPIN1 (I/O bit 1)	-	-
21	IOPIN2 (I/O bit 2)	-	-
22	IOPIN3 (I/O bit 3)	-	-
23	IOPIN4 (I/O bit 4)	-	-
24	IOPIN5 (I/O bit 5)	-	-
25	IOPIN6 (I/O bit 6)	-	-
26	IOPIN7 (I/O bit 7)	-	-
27	27 Vcc (5V/100mA max) ⁽²⁾	-	-
28	28 Vsens+ (+15V/1mA max) ⁽²⁾	-	-
29	29 Vsens- (-15V/1mA max) ⁽²⁾	-	-
30	GND	-	-
31	TRIGGER	-	-
32	DGND	-	-

⁽¹⁾16 input channels only available using DAQ i116/i250/i516/i616

⁽²⁾Sensor power supply

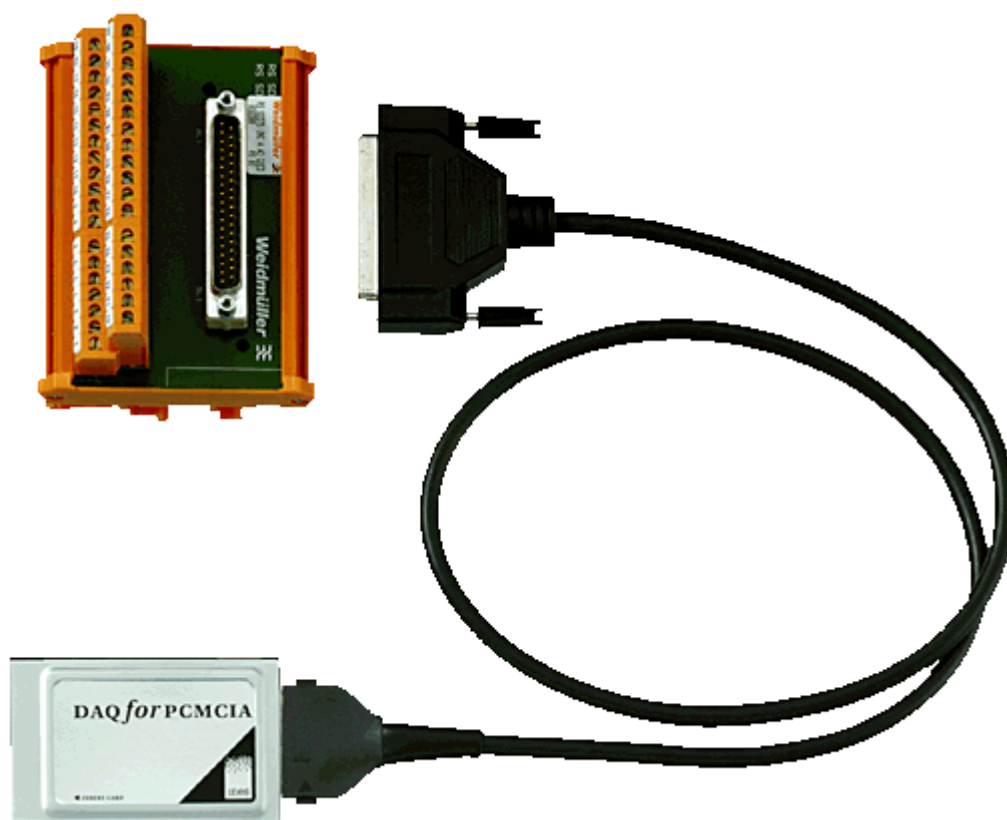
Pin 1 position

Card is held with "DAQ for PCMCIA" label on top side. Then look "into" connector (flat gold pins are upside down).

Under these conditions, pin32 is left and pin1 is right.

Accessories for data acquisition cards

Terminal box



A terminal box and DSUB cable are available separately. If this terminal box is used, there are pin numbers directly at the screw terminals. These numbers are identical to the pin assignments above; the cable does not change any assignment.

Strain relief assembly



The end of flimsy PC-Card connectors! In the past, the flimsy PC-Cards connector was the most important problem in using this smart

technology in Test and Measurement application. With the Ruggedized Strain Relief Assembly (SRA-1 Kit), the PC-Card technology becomes a professional solution for Test and Measurement. The SRA-1 Kit is designed for a permanent and mechanically durable connection between PC-Card and cable. After both parts are connected, they can be detached by disassembly of the SRA-1 only. Stainless steel construction!

Cable with open wire outlet



Shielded cable (1m) with 1 HIROSE connector (card side) and open wire outlet (stripped wire ends) on other side for user-built cables or direct sensor attachment.

Hardware Specifications

General

Card types: Series of data acquisition cards with 1 A/D converter with 12 bit resolution and 8 bit digital port:

- DAQ i108 PCMCIA (100kHz, 8 channels)
- DAQ i116 PCMCIA (100kHz, 16 channels)
- DAQ i250 PCMCIA (250kHz, 16 channels)
- DAQ i508 PCMCIA (500kHz, 8 channels)
- DAQ i516 PCMCIA (500kHz, 16 channels)
- DAQ i608 PCMCIA (625kHz, 8 channels)
- DAQ i616 PCMCIA (625kHz, 16 channels)

Compliance: PCMCIA release 2.1, type II PC-Card

Environment: Temperature 0...50 C, humidity < 80 % non-condensing (all parameters are specified for 25 C)

Power consumption: 1.25W (5V/250mA) typ. while active, 0.25W (5V/50mA) typ. while in sleep mode

Sensor power supply: +15V/1mA, -15V/1mA, +5V/100mA

Analog inputs

Inputs: DC coupled

- DAQ i108 /i508/i608 : 8 single ended channels or 4 differential
- DAQ i116/i250/i516/i616 : 16 single ended channels or 8 differential DC coupling.

ADC Resolution: 12 bit

Input ranges: Input mode (single ended or differential) and ranges are selectable by software.

- 8 Unipolar ranges: +1.25V, +2.5V, +3.75V, +5V, +6.25V, +7.5V, +8.75V, +10V
- 16 Bipolar ranges: +/-0.625V, +/-1.25V, +/-1.875, +/-2.5V, +/-3.125V, +/-3.75V, +/-4.375V, +/-5V, +/-5.625V, +/-6.25V, +/-6.875V, +/-7.5V, +/-8.125V, +/-8.75V, +/-9.375V, +/-10V

Sample rate: Timing hardware-controlled, +/-0.5% initial tolerance

- DAQ i108 / i116 : 305.1Hz to 100kHz (<=32 kHz sample rate recommended if multiple channel acquisition is performed).
- DAQ i250 : 305.1Hz to 250kHz (<=90 kHz sample rate recommended if multiple channel acquisition is performed).
- DAQ i508 / i516 : 305.1Hz to 500kHz (<=175kHz recommended if multiple channel acquisition is performed).
- DAQ i608 / i616 : 305.1Hz to 625kHz (646kHz setting not guaranteed, <=175kHz sample rate recommended if multiple channel acquisition is performed).

Anti aliasing filter: 1 pole RC-type lowpass filter. Cutoff frequency can be modified by external resistor. -3db cutoff frequency is:

- DAQ i108 : 50kHz +/-20%, roll-off 40db/decade
- DAQ i250 : 120kHz +/-20% , roll-off 40db/decade
- DAQ i508 / i516 / i608 / i616 : 300kHz +/-20%, roll-off 60db/decade

Input bandwidth: 250kHz typ. (DAQ i250: 125kHz)

AtoD DNL: +/-1.0 LSB typ.

AtoD INL: +/-1.0 LSB typ.

Gain accuracy: 1% at 55ppm/K drift

Settling time: < 2us to 1 LSB, full scale step input

Temperature coefficient of reference voltage: < +/-45 ppm/K

Input impedance:

- DAQ i508 /i516/i608/i616: >10MOhms for input frequencies < 250kHz , single-ended input
- DAQ i108 /i116/i250: >10MOhms at DC level, approx. (4000+10E9/Fin) Ohms for AC (24kOhms at 50kHz)

Trigger facilities: Programmable threshold, 8 bit resolution.

Pretrigger: 1 to 16383 samples

Trigger events: Cross of threshold level, rising (positive) edge or falling (negative) edge.

Input voltage above or below threshold level. Hardware controlled event detection.

Sample buffer: 32kByte (16384 samples)

Acquisition modes:

- Single capture mode for sampling at low rates
- Trigger mode for event detection
- Continuous acquisition (FIFO) mode

Protection: All analog inputs are protected to 35V relative to card's ground.

Digital port

Digital I/O: 8 bit bi-directional

Port type: CMOS drivers, 4 mA drive capability to TTL-level

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